Section 39. Oscillator (Part III)

HIGHLIGHTS

This section of the manual contains the following topics:

Note: This family reference manual section is meant to serve as a complement to device data sheets. Depending on the device variant, this manual section may not apply to all dsPIC33F/PIC24H devices.

Please consult the note at the beginning of the **"Oscillator Configuration"** chapter in the current device data sheet to check whether this document supports the device you are using.

Device data sheets and family reference manual sections are available for download from the Microchip Worldwide Web site at: http://www.microchip.com.

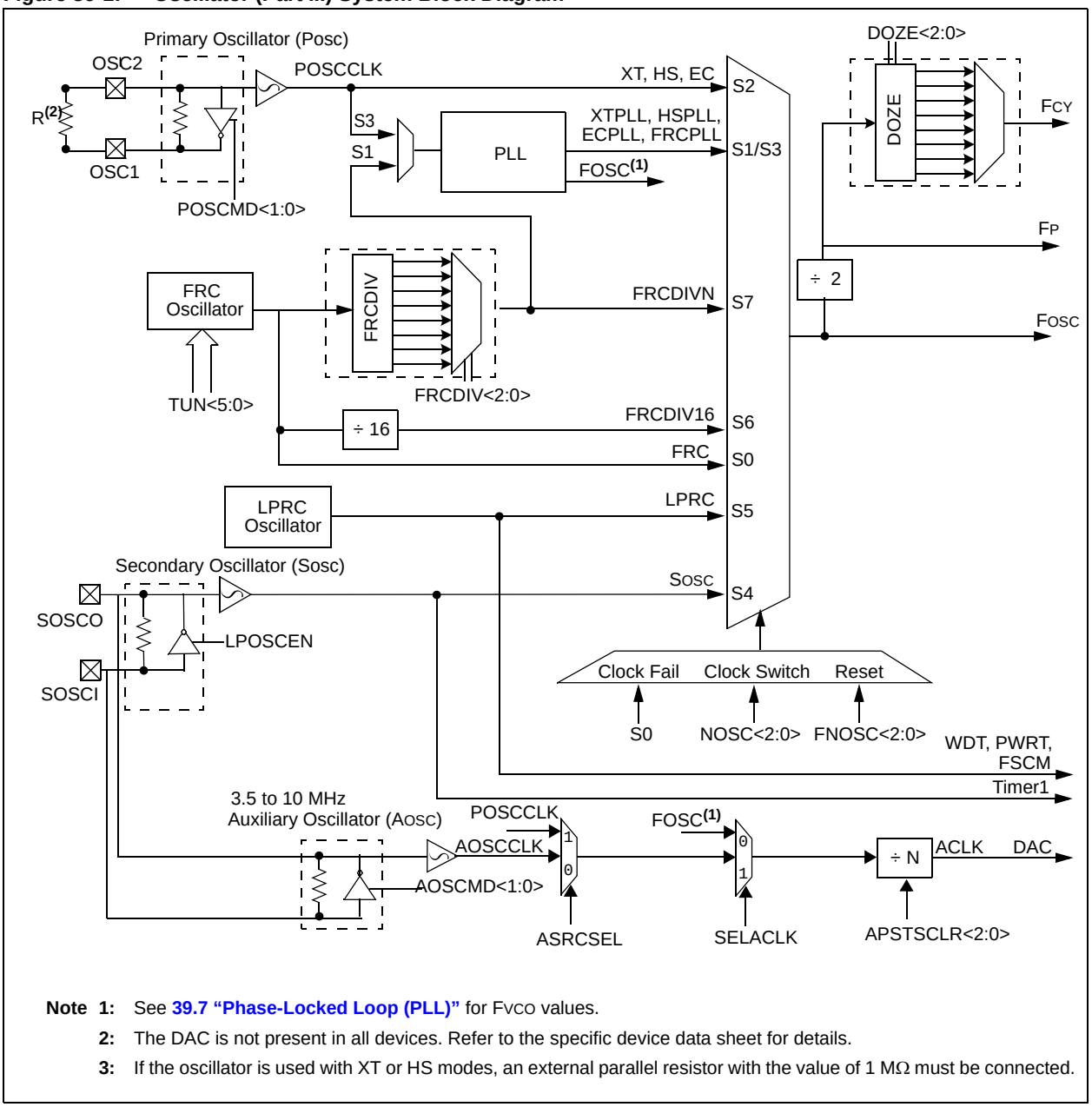
39.1 INTRODUCTION

The dsPIC33F/PIC24H oscillator system includes these characteristics:

- External and internal oscillator options
- On-chip Phase-Locked Loop (PLL) to boost the internal operating frequency on selected internal and external oscillator sources
- On-the-fly clock switching between various clock sources
- Doze mode for system power-saving
- Fail-Safe Clock Monitor (FSCM) that detects clock failure and permits safe application recovery or shutdown
- Nonvolatile Configuration bits for clock source selection
- Auxiliary Crystal Oscillator for Digital-to-Analog Converter (DAC)

A block diagram of the dsPIC33F/PIC24H oscillator system is shown in Figure 39-1.

Figure 39-1: Oscillator (Part III) System Block Diagram



Note 1: See **39.7 "Phase-Locked Loop (PLL)"** for FVCO values.

2: The DAC is not present in all devices. Refer to the specific device data sheet for details.

3: If the oscillator is used with XT or HS modes, an external parallel resistor with the value of 1 MΩ must be connected.

39.2 CPU CLOCKING

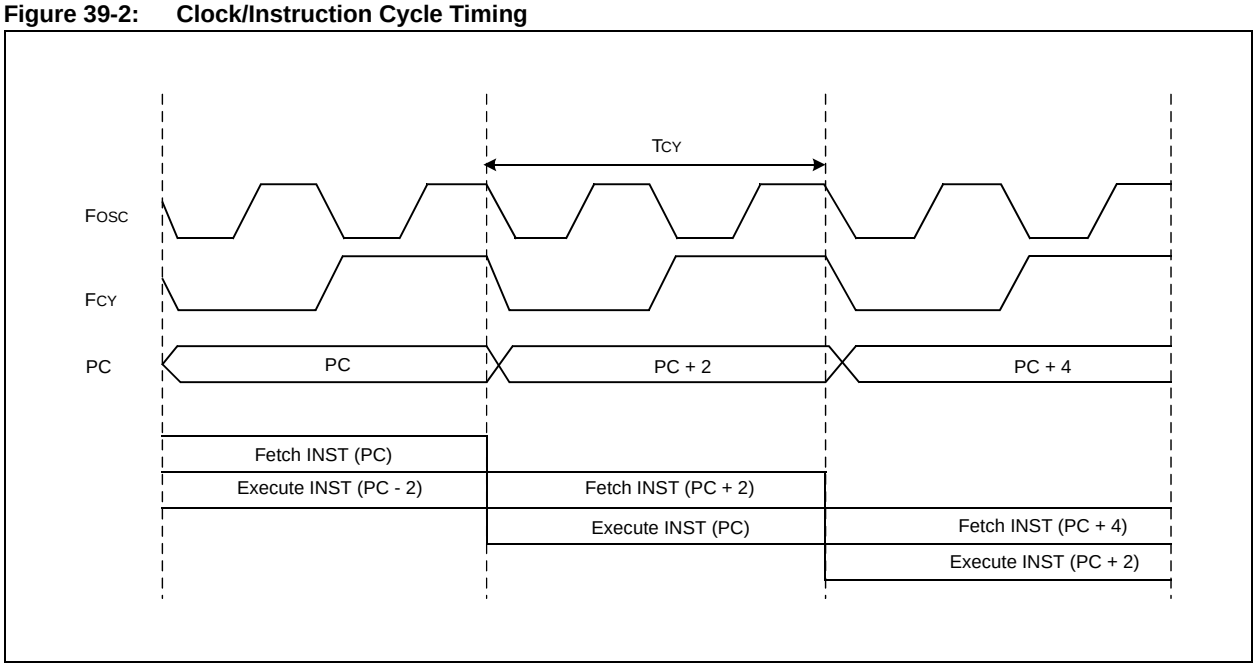
The system clock (FOSC) source can be provided by one of the following options:

- Primary Oscillator (POSC) on the OSC1 and OSC2 pins
- Secondary Oscillator (SOSC) on the SOSCI and SOSCO pins
- Internal Fast RC (FRC) Oscillator with optional clock divider
- Internal Low-Power RC (LPRC) Oscillator
- POSC with PLL
- Internal Fast RC Oscillator with PLL

The FOSC source is divided by 2 to produce the internal instruction cycle clock. The instruction cycle clock is denoted by FCY. The timing diagram in Figure 39-2 shows the relationship among the system clock (FOSC), instruction cycle clock (FCY), and Program Counter (PC).

FCY can be output on the OSC2 I/O pin if the Primary Oscillator mode or the High Speed Oscillator (HS) mode is not selected as the clock source (see **39.5 "Primary Oscillator (Posc)"**).

Figure 39-2: Clock/Instruction Cycle Timing



39.3 OSCILLATOR CONFIGURATION REGISTERS

Oscillator Configuration registers are located in the program memory space, and are not Special Function Registers (SFRs). These two registers are mapped into program memory space and are programmed at the time of device programming.

- **FOSCSEL: Oscillator Source Selection Register**

  The FOSCSEL register selects the initial oscillator source and start-up option. FOSCSEL contains the following Configuration bit:

  The Initial Oscillator Source Selection Configuration bits (FNOSC<2:0>) in the Oscillator Source Selection register (FOSCSEL<2:0>) determine the clock source that is used at a Power-on Reset (POR). Thereafter, the clock source can be changed between permissible clock sources with clock switching.

  The Internal FRC Oscillator with postscaler (FRCDIVN) is the default (unprogrammed) selection.

- **FOSC: Oscillator Configuration Register**

  The FOSC register configures the Primary Oscillator mode, OSCO pin function, peripheral pin select, and the fail-safe and clock switching modes. FOSC contains the following Configuration bits:

  - The Primary Oscillator Mode Selection Configuration bits (POSCMD<1:0> in the Oscillator Configuration Register (FOSC<1:0>)select the operation mode of the POSC.
  - The OSC2 Pin Function (OSCIOFNC) configuration bit in the Oscillator Configuration Register (FOSC<2>) selects the OSC2 pin function, except in HS or Medium-Speed Oscillator (XT) mode.

    When OSCIOFNC is unprogrammed (‘1’), the FCY clock is output on the OSC2 pin.

    When OSCIOFNC is programmed (‘0’), the OSC2 pin becomes a general purpose I/O pin.

Table 39-1 lists the configuration settings that select the device oscillator source and operating mode at a POR.

Table 39-1: Configuration Bit Values for Clock Selection

Oscillator Source	Oscillator Mode	FNOSC Value	POSCMD Value	Note
S0	Fast RC (FRC) Oscillator	000	xx	**1**
S1	Fast RC Oscillator with PLL (FRCPLL)	001	xx	**1**
S2	Primary Oscillator (EC)	010	00	**1**
S2	Primary Oscillator (XT)	010	01	—
S2	Primary Oscillator (HS)	010	10	—
S3	Primary Oscillator with PLL (ECPLL)	011	00	**1**
S3	Primary Oscillator with PLL (XTPLL)	011	01	—
S3	Primary Oscillator with PLL (HSPLL)	011	10	—
S4	Secondary Oscillator (SOSC)	100	xx	**1**
S5	Low-Power RC (LPRC) Oscillator	101	xx	**1**
S6	Fast RC Oscillator with Divide-by-16 (FRCDIV16)	110	xx	**1**
S7	Fast RC Oscillator with Divide-by-N (FRCDIVN)	111	xx	**1, 2**

Note 1: The OSC2 pin function is determined by the OSCIOFNC Configuration bit.

2: The default oscillator mode for an unprogrammed (erased) device.

Register 39-1: FOSCSEL: Oscillator Source Selection Register

U	U	U	U	U	U	U	U
—	—	—	—	—	—	—	—
bit 15							bit 8

R/P	U	U	U	U	R/P	R/P	R/P
IESO	—	—	—	—	FNOSC<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as ‘1’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘1’

bit 7 **IESO:** Internal External Start-up Option bit

1 = Start-up device with the Internal FRC Oscillator, and then automatically switch to the user-selected oscillator source when ready

0 = Start-up device with user-selected oscillator source

bit 6-3 **Unimplemented:** Read as ‘1’

bit 2-0 **FNOSC<2:0>:** Initial Oscillator Source Selection bits

111 = Fast RC (FRC) Oscillator with Divide-by-N (FRCDIVN)

110 = Fast RC Oscillator with Divide-by-16 (FRCDIV16)

101 = Low-Power RC (LPRC) Oscillator

100 = Secondary Oscillator (SOSC)

011 = Primary Oscillator with PLL (XTPLL, HSPLL, ECPLL)

010 = Primary Oscillator (XT, HS, EC)

001 = Fast RC Oscillator with PLL (FRCPLL)

000 = Fast RC Oscillator (FRC)

Register 39-2: FOSC: Oscillator Configuration Register

U	U	U	U	U	U	U	U
—	—	—	—	—	—	—	—
bit 15							bit 8

R/P	R/P	R/P	U	U	R/P	R/P	R/P
FCKSM<1:0>		IOL1WAY(1)	—	—	OSCIOFNC	POSCMD<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '1'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '1'

bit 7-6 **FCKSM<1:0>:** Clock Switching Mode bits
1x = Clock switching is disabled, Fail-Safe Clock Monitor (FSCM) is disabled
01 = Clock switching is enabled, FSCM is disabled
00 = Clock switching is enabled, FSCM is enabled

bit 5 **IOL1WAY:** Peripheral Pin Select Configuration bit(1)
1 = Allow only one reconfiguration
0 = Allow multiple reconfigurations

bit 4-3 **Unimplemented:** Read as '1'

bit 2 **OSCIOFNC:** OSC2 Pin Function bit (except in XT and HS modes)
1 = OSC2 is clock output and instruction cycle (FCY) clock is output on OSC2 pin
0 = OSC2 is a general purpose digital I/O pin

bit 1-0 **POSCMD<1:0>:** Primary Oscillator Mode Selection bits
11 = Primary Oscillator (POSC) disabled
10 = HS (High-Speed) Crystal Oscillator mode
01 = XT (Crystal) Oscillator mode
00 = EC (External Clock) mode

Note 1: The IOL1WAY bit is not available on all devices. Refer to the **"Oscillator Configuration"** chapter in the specific device data sheet for more information.

39.4 SPECIAL FUNCTION REGISTERS

The following Special Function Registers (SFRs) provide run-time control and status of the oscillator system:

- **OSCCON: Oscillator Control Register**

  OSCCON controls clock switching and provides status information that allows current clock source, PLL lock, and clock fail conditions to be monitored.

- **CLKDIV: Clock Divisor Register**

  CLKDIV controls Doze mode and selects a PLL prescaler, a PLL postscaler, and an FRC postscaler.

- **PLLFBD: PLL Feedback Divisor Register**

  PLLFBD selects the PLL feedback divisor.

- **OSCTUN: FRC Oscillator Tuning Register**

  OSCTUN is used to tune the Internal FRC Oscillator frequency in software. It allows the Internal FRC Oscillator frequency to be adjusted over a range of ±12%.

- **ACLKCON: Auxiliary Clock Control Register**

  ACLKCON controls the Auxiliary Oscillator mode and the auxiliary output clock divider.

Note:	The Oscillator SFRs (OSCCON, CLKDIV, PLLFBD, OSCTUN and ACLKCON) are reset only on a POR.

Register 39-3: OSCCON: Oscillator Control Register

U-0	R-y	R-y	R-y	U-0	R/W-y	R/W-y	R/W-y
—	COSC<2:0>			—	NOSC<2:0>		
bit 15							bit 8

R/S-0	R/W-0	R-0	U-0	R/C-0	U-0	R/W-0	R/W-0
CLKLOCK	IOLOCK(1)	LOCK	—	CF	—	LPOSCEN	OSWEN
bit 7							bit 0

Legend:	U= Unimplemented bit, read as '0'	y = Depends on FOSCSEL<FNOSC> bits	
R = Readable bit	W = Writable bit	C = Clearable only bit	S = Settable only bit
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **COSC<2:0>:** Current Oscillator Selection bits (read-only)
111 = Fast RC (FRC) Oscillator with Divide-by-N (FRCDIVN)
110 = Fast RC Oscillator with Divide-by-16 (FRCDIV16)
101 = Low-Power RC (LPRC) Oscillator
100 = Secondary Oscillator (SOSC)
011 = Primary Oscillator (POSC) with PLL (XTPLL, HSPLL, ECPLL)
010 = Primary Oscillator (XT, HS, EC)
001 = Fast RC Oscillator with PLL (FRCPLL)
000 = Fast RC Oscillator (FRC)

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **NOSC<2:0>:** New Oscillator Selection bits
111 = Fast RC(FRC) Oscillator with Divide-by-N (FRCDIVN)
110 = Fast RC Oscillator with Divide-by-16 (FRCDIV16)
101 = Low-Power RC (LPRC) Oscillator
100 = Secondary Oscillator (SOSC)
011 = Primary Oscillator (POSC) with PLL (XTPLL, HSPLL, ECPLL)
010 = Primary Oscillator (XT, HS, EC)
001 = Fast RC Oscillator with PLL (FRCPLL)
000 = Fast RC Oscillator (FRC)

bit 7 **CLKLOCK:** Clock Lock Enable bit
If clock switching is enabled and FSCM is disabled (FOSC<7:6> = 01):
1 = Clock switching is disabled, system clock source is locked
0 = Clock switching is enabled, system clock source may be modified by clock switching

bit 6 **IOLOCK:** Peripheral Pin Select Lock bit(1)
1 = Peripheral Pin Select is locked. Writes to the Peripheral Pin Select registers are not allowed.
0 = Peripheral Pin Select is not locked. Writes to the Peripheral Pin Select registers are allowed.

bit 5 **LOCK:** PLL Lock Status bit (read-only)
1 = Indicates that PLL is in lock, or PLL start-up timer is satisfied
0 = Indicates that PLL is out of lock, start-up timer is in progress or PLL is disabled

bit 4 **Unimplemented:** Read as '0'

Note 1: The IOLOCK bit is not available on all devices. Refer to the **"Oscillator Configuration"** chapter in the specific device data sheet for more information.

Note: Writes to this register require an unlock sequence. Refer to **39.12 "Clock Switching"** for details and examples.

Register 39-3: OSCCON: Oscillator Control Register (Continued)

bit 3 **CF:** Clock Fail Detect bit (read/clear by application)
1 = FSCM has detected clock failure
0 = FSCM has not detected clock failure

bit 2 **Unimplemented:** Read as '0'

bit 1 **LPOSCEN:** Secondary Oscillator (SOSC) Enable bit
1 = Enable Secondary Oscillator
0 = Disable Secondary Oscillator

bit 0 **OSWEN:** Oscillator Switch Enable bit
1 = Request oscillator switch to selection specified by NOSC<2:0> bits
0 = Oscillator switch is complete

Note 1: The IOLOCK bit is not available on all devices. Refer to the **"Oscillator Configuration"** chapter in the specific device data sheet for more information.

Note: Writes to this register require an unlock sequence. Refer to **39.12 "Clock Switching"** for details and examples.

Register 39-4: CLKDIV: Clock Divisor Register

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
ROI	DOZE<2:0>			DOZEN(1)	FRCDIV<2:0>		
bit 15							bit 8

R/W-0	R/W-1	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PLLPOST<1:0>		—	PLLPRE<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ROI:** Recover On Interrupt bit
1 = Interrupts clear the DOZEN bit and the processor clock/peripheral clock ratio is set to 1:1
0 = Interrupts have no effect on the DOZEN bit

bit 14-12 **DOZE<2:0>:** Processor Clock Reduction Select bits(2)
111 = FCY divided by 128
110 = FCY divided by 64
101 = FCY divided by 32
100 = FCY divided by 16
011 = FCY divided by 8 (default)
010 = FCY divided by 4
001 = FCY divided by 2
000 = FCY divided by 1

bit 11 **DOZEN:** DOZE Mode Enable bit(1,2)
1 = DOZE<2:0> field specifies the ratio between the peripheral clocks and the processor clocks
0 = Processor clock/peripheral clock ratio forced to 1:1

bit 10-8 **FRCDIV<2:0>:** Internal Fast RC Oscillator Postscaler bits
111 = FRC divided by 256
110 = FRC divided by 64
101 = FRC divided by 32
100 = FRC divided by 16
011 = FRC divided by 8
010 = FRC divided by 4
001 = FRC divided by 2
000 = FRC divided by 1 (default)

bit 7-6 **PLLPOST<1:0>:** PLL VCO Output Divider Select bits (also denoted as 'N2', PLL postscaler)
11 = Output divided by 8
10 = Reserved
01 = Output divided by 4 (default)
00 = Output divided by 2

bit 5 **Unimplemented:** Read as '0'

bit 4-0 **PLLPRE<4:0>:** PLL Phase Detector Input Divider Select bits (also denoted as 'N1', PLL prescaler)
11111 = Input/33
•
•
•
00001 = Input divided by 3
00000 = Input divided by 2 (default)

Note 1: This bit is cleared when the ROI bit is set and an interrupt occurs.

2: For more information on Doze mode, refer to **Section 9. "Watchdog Timer and Power-Saving Modes"** (DS70196).

Register 39-5: PLLFBD: PLL Feedback Divisor Register

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	PLLDIV<8>
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
PLLDIV<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-9 **Unimplemented:** Read as '0'

bit 8-0 **PLLDIV<8:0>:** PLL Feedback Divisor bits (also denoted as 'M', PLL multiplier)

111111111 = 513
•
•
•
000110000 = 50 (default)
•
•
•
000000010 = 4
000000001 = 3
000000000 = 2

Register 39-6: OSCTUN: FRC Oscillator Tuning Register

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	TUN<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as '0'

bit 5-0 **TUN<5:0>:** FRC Oscillator Tuning bits

011111 = Center frequency + 11.625% (8.23 MHz)
011110 = Center frequency + 11.25% (8.20 MHz)
•
•
•
000001 = Center frequency + 0.375% (7.40 MHz)
000000 = Center frequency (7.37 MHz nominal)
111111 = Center frequency - 0.375% (7.345 MHz)
•
•
•
100001 = Center frequency - 11.625% (6.52 MHz)
100000 = Center frequency - 12% (6.49 MHz)

Register 39-7: ACLKCON: Auxiliary Clock Control Register

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	SELACLK	AOSCMD<1:0>		APSTSCLR<2:0>		
bit 15							bit 8

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
ASRCSEL	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13 **SELACLK:** Select Auxiliary Clock Source for Auxiliary Clock Divider bit
1 = Auxiliary Oscillator (AOSC) provides the source clock for Auxiliary Clock Divider
0 = PLL output provides the source clock for Auxiliary Clock Divider

bit 12-11 **AOSCMD<1:0>:** Auxiliary Oscillator Mode bits
11 = EC (External Clock) Mode Select
10 = XT (Crystal) Oscillator Mode Select
01 = HS (High-Speed) Oscillator Mode Select
00 = Auxiliary Oscillator (AOSC) Disabled (default)

bit 10-8 **APSTSCLR<2:0>:** Auxiliary Clock Output Divider bits
111 = Divided by 1
110 = Divided by 2
101 = Divided by 4
100 = Divided by 8
011 = Divided by 16
010 = Divided by 32
001 = Divided by 64
000 = Divided by 256 (default)

bit 7 **ASRCSEL:** Select Reference Clock Source for Auxiliary Clock bit
1 = Primary Oscillator (POSC) is the clock source
0 = Auxiliary Oscillator (AOSC) is the clock source

bit 6-0 **Unimplemented:** Read as ‘0’

39.5 PRIMARY OSCILLATOR (POSC)

The Primary Oscillator (POSC) is available on the OSC1 and OSC2 pins of the dsPIC33F/PIC24H device families. This connection enables an external crystal (or ceramic resonator) to provide the clock to the device. Optionally, the POSC can be used with the internal PLL to boost the FOSC to 80 MHz for 40 MIPS execution. The POSC provides the following modes of operation:

- **Medium-Speed Crystal Oscillator (XT Mode)**

  XT mode is a medium-gain, medium-frequency mode used to work with crystal frequencies of 3-10 MHz.

- **High-Speed Oscillator (HS Mode)**

  HS mode is a high-gain, high-frequency mode that is used to work with crystal frequencies of 10-40 MHz.

- **External Clock Source Operation (EC Mode)**

  If the on-chip oscillator is not used, EC mode allows the internal oscillator to be bypassed. The device clocks are generated from an external source (0.8-64 MHz) and input on the OSC1 pin.

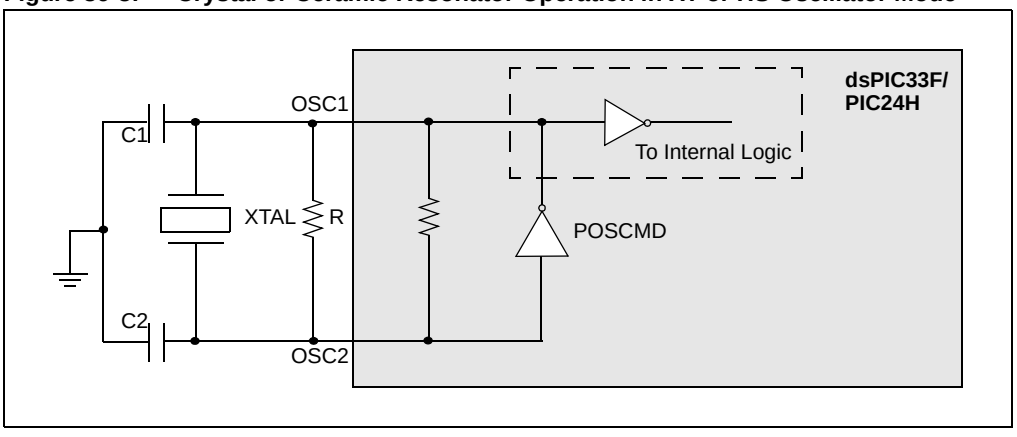
The Initial Oscillator Source Selection Configuration bits (FNOSC<2:0>) in the Oscillator Source Selection register (FOSCSEL<2:0>) specify the POSC clock source at a POR. The Primary Oscillator Mode Selection Configuration bits (POSCMD<1:0>) in the Oscillator Configuration register (FOSC<1:0>) specify the Primary Oscillator mode. Table 39-2 shows the options selected by specific bit configurations, which are programmed at the time of device programming.

Table 39-2: Primary Oscillator Clock Source Options

FNOSC Value	POSCMD	Primary Oscillator Source/Mode
010	00	Primary Oscillator: External Clock Mode (EC)
010	01	Primary Oscillator: Medium Frequency Mode (XT)
010	10	Primary Oscillator: High-Frequency Mode (HS)
011	00	Primary Oscillator with PLL: External Clock Mode (ECPLL)
011	01	Primary Oscillator with PLL: Medium-Frequency Mode (XTPLL)
011	10	Primary Oscillator with PLL: High-Frequency Mode (HSPLL)

Figure 39-3 shows a recommended crystal oscillator circuit diagram for dsPIC33F/PIC24H devices. Capacitors C1 and C2 form the load capacitance for the crystal. The optimum load capacitance (CL) for a given crystal is specified by the crystal manufacturer. Load capacitance can be calculated as shown in Equation 39-1.

Figure 39-3: Crystal or Ceramic Resonator Operation in XT or HS Oscillator Mode



Capacitors C1 and C2 form the load capacitance for the crystal.

Equation 39-1: Crystal Load Capacitance

$$C_L = C_S + \frac{C1 \cdot C2}{C1 + C2}$$

Where:

C_S is the stray capacitance

Assuming $C1 = C2$, Equation 39-2 gives the capacitor value (C1, C2) for a given load and stray capacitance.

Equation 39-2: External Capacitor for Crystal

$$C1 = C2 = 2 \cdot (C_L - C_S)$$

For additional information on crystal oscillators and their operation, refer to **39.15 "Related Application Notes"**.

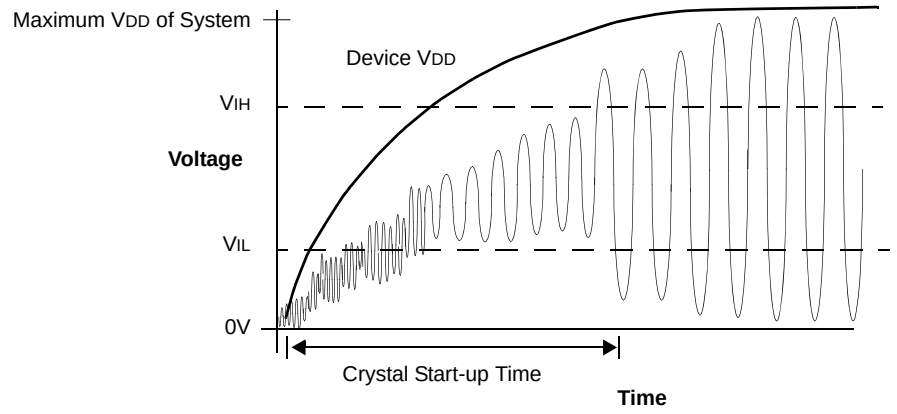
39.5.1 Oscillator Start-up Time

The oscillator starts oscillating as the device voltage increases from VSS. The time required for the oscillator to start oscillating depends on the following factors:

- Crystal/Resonator frequency
- Capacitor values used (C1 and C2 in Figure 39-3)
- Device VDD rise time
- System temperature
- Series resistor value and type if used
- Oscillator mode selection of device (selects the gain of the internal oscillator inverter)
- Crystal quality
- Oscillator circuit layout
- System noise

Figure 39-4 shows a plot of a typical oscillator and resonator start-up.

Figure 39-4: Example Oscillator and Resonator Start-up Characteristics



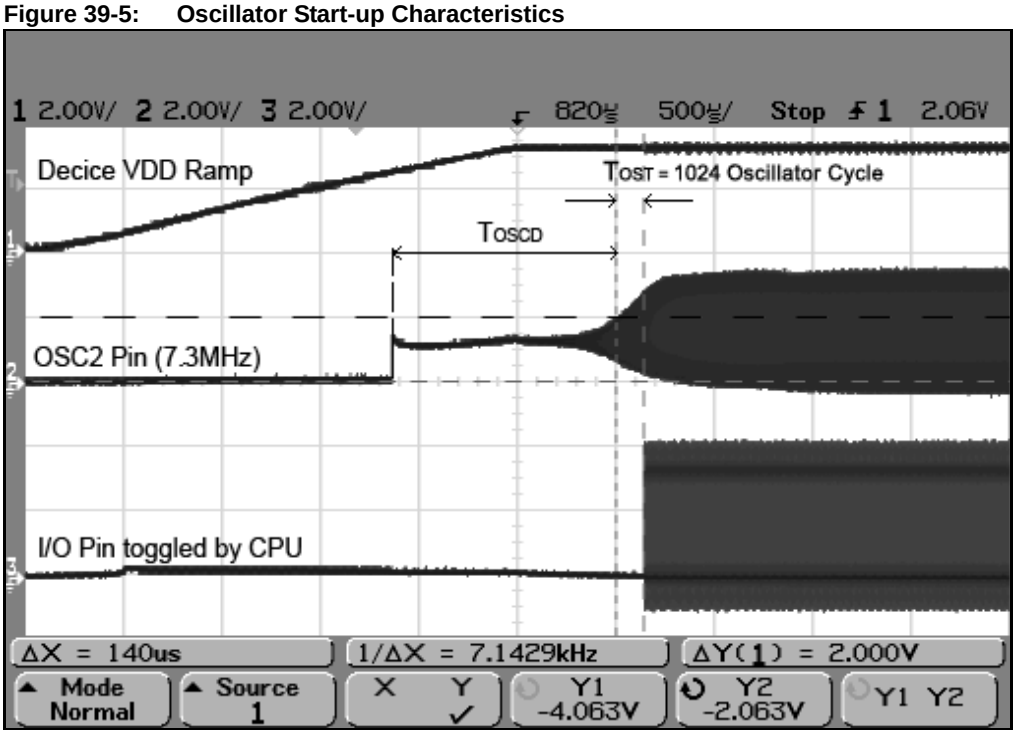
To ensure that a crystal oscillator (or ceramic resonator) has started and stabilized, an Oscillator Start-up Timer (OST) is provided with the POSC and the SOSC. The OST is a simple 10-bit counter that counts 1024 cycles before releasing the oscillator clock to the rest of the system. This time-out period is denoted as TOST.

The amplitude of the oscillator signal must reach the VIL and VIH thresholds for the oscillator pins before the OST can begin to count cycles. The TOST interval is required every time the oscillator restarts (e.g., on POR, BOR, and wake-up from Sleep mode).

When the POSC is enabled, it takes a finite amount of time to start oscillating. This delay is denoted as TOSCD. After TOSCD, the OST timer takes 1024 clock cycles (TOST) to release the clock. The total delay for the clock to be ready is TOSCD + TOST. If the PLL is used, an additional delay is required for the PLL to lock (see **39.7 "Phase-Locked Loop (PLL)"**).

POSC start-up behavior is illustrated in Figure 39-5, indicating where the CPU begins toggling an I/O pin when it starts execution after the TOSCD + TOST interval.

Figure 39-5: Oscillator Start-up Characteristics



39.5.2 POSC Pin Functionality

The POSC pins (OSC1/OSC2) can be used for other functions when the oscillator is not being used.

The POSCMD Configuration bits (POSCMD<1:0>) in the Oscillator Configuration register (FOSC<1:0>) determine the following oscillator pin function.

POSCMD: Primary Oscillator Mode Selection bits:

- 11 = Primary Oscillator mode disabled
- 10 = HS Oscillator mode selected
- 01 = XT Oscillator mode selected
- 00 = External Clock mode selected

The OSCIOFNC bit (FOSC<2>) determines the following OSC2 pin function.

OSCIOFNC: OSC2 Pin Function bit (except in XT and HS modes):

- 1 = OSC2 is the clock output and the instruction cycle (FCY) clock is output on the OCS2 pin, see Figure 39-6
- 0 = OSC2 is a general purpose digital I/O pin, see Figure 39-7

The oscillator pin functions are shown in Table 39-3.

Table 39-3: Clock Pin Function Selection

Oscillator Source	OSCIOFNC Value	POSCMD<1:0> Value	OSC1(1) Pin Function	OSC2(2) Pin Function
POSC Disabled	1	11	Digital I/O	Clock Output (FCY)
POSC Disabled	0	11	Digital I/O	Digital I/O
HS (High-Speed)	X	10	OSC1	OSC2
XT (Crystal)	X	01	OSC1	OSC2
EC (External Clock)	1	00	OSC1	Clock Output (FCY)
EC (External Clock)	0	00	OSC1	Digital I/O

Note 1: OSC1 pin function is determined by the Primary Oscillator Mode Configuration bits (POSCMD<1:0>).

2: OSC2 pin function is determined by Primary Oscillator Mode Configuration bits (POSCMD<1:0>) and OSC2 Pin Function Configuration bits (OSCIOFNC<2>).

Figure 39-6: OSC2 Pin for Clock Output (in EC Mode), FOSC<2> = 1

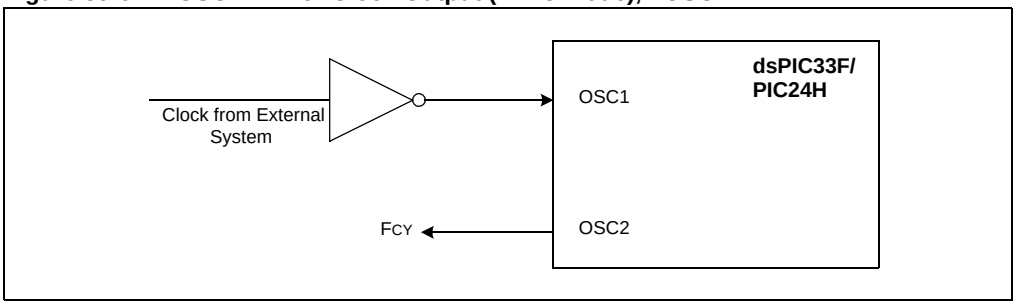
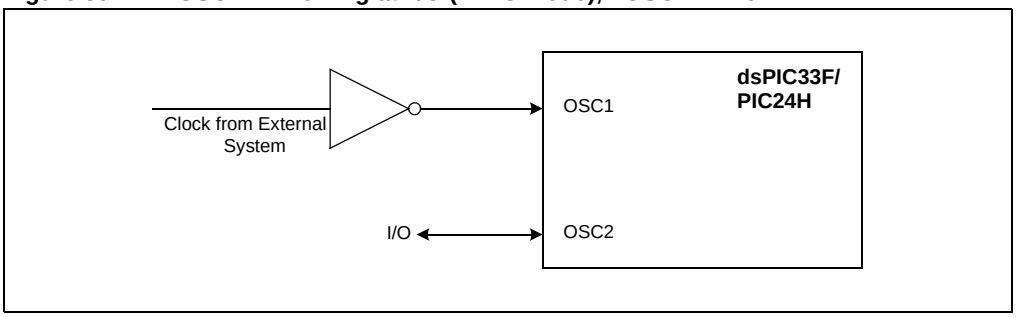


Figure 39-7: OSC2 Pin for Digital I/O (in EC Mode), FOSC<2> = 0



39.6 INTERNAL FAST RC (FRC) OSCILLATOR

The Internal Fast RC (FRC) Oscillator provides a nominal 7.37 MHz clock without requiring an external crystal or ceramic resonator, which results in system cost savings for applications that do not require a precise clock reference.

The application software can tune the frequency of the oscillator from -12% to +11.625% (30 kHz steps) of the nominal frequency value using the FRC Oscillator Tuning bits (TUN<5:0>) in the FRC Oscillator Tuning register (OSCTUN<5:0>).

Note 1: Refer to the **"Oscillator Configuration"** chapter in the specific device data sheet for the accuracy of the FRC clock frequency over temperature and voltage variations.

2: The FRC Oscillator Tuning bits (TUN<5:0>) should not be changed dynamically when operating in internal FRC with PLL. To change the FRC Oscillator Tuning bits:

a) Switch the clock to a non-PLL mode (e.g., Internal FRC).

b) Make the necessary changes.

c) Switch the clock back to the PLL mode.

The Internal FRC Oscillator starts up instantly. Unlike a crystal oscillator, which can take several milliseconds to begin oscillation, the Internal FRC Oscillator starts oscillating immediately.

The Initial Oscillator Source Selection Configuration bits (FNOSC<2:0>) in the Oscillator Source Selection register (FOSCSEL<2:0>) select the FRC clock source. The Internal FRC Oscillator clock source options at the time of a POR are shown in Table 39-4. The Configuration bits are programmed at the time of device programming.

Table 39-4: Internal FRC Oscillator Clock Source Options at POR

FNOSC<2:0> Value	POSC Source/Mode
111	FRC Oscillator: Postscaler by N (FRCDIVN)
110	FRC Oscillator: Postscaler by 16 (FRCDIV16)
001	FRC Oscillator with PLL (FRCPLL)
000	FRC Oscillator (FRC)

39.6.1 Internal FRC Oscillator Postscaler Mode (FRCDIVN)

In the Internal FRC Oscillator Postscaler mode, a variable postscaler divides the FRC clock output and allows a lower frequency to be chosen. The postscaler is controlled by the Internal Fast RC Oscillator Postscaler bits (FRCDIV<2:0>) in the Clock Divisor register (CLKDIV<10:8>). These bits allow eight settings, from 1:1 to 1:256, to be chosen, as shown in Table 39-5.

Table 39-5: Internal FRC Oscillator Postscaler Settings

FRCDIV<2:0> Value	Internal FRC Oscillator Setting
111	FRC divide by 256
110	FRC divide by 64
101	FRC divide by 32
100	FRC divide by 16
011	FRC divide by 8
010	FRC divide by 4
001	FRC divide by 2
000	FRC divide by 1 (default)

Optionally, the FRC postscaler output can be used with the internal PLL to boost the system frequency (FOSC) to 80 MHz for 40 MIPS instruction cycle execution speed.

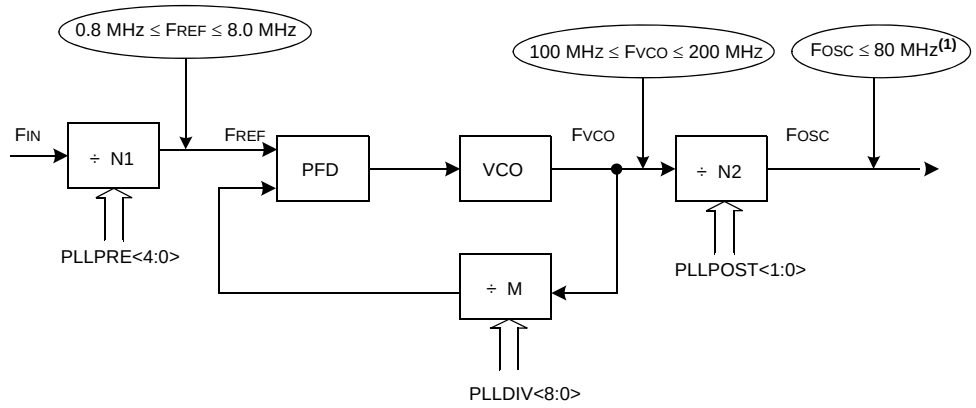
Note: The FRC divider should not be changed dynamically when operating in Internal FRC with PLL. To change the FRC divider:

1. Switch the clock to non-PLL mode (for example, Internal FRC).
2. Make the necessary changes.
3. Switch the clock back to the PLL mode.

39.7 PHASE-LOCKED LOOP (PLL)

The POSC and Internal FRC Oscillator sources can optionally use an on-chip PLL to obtain higher operating speeds. A block diagram of the PLL module is shown in Figure 39-8.

Figure 39-8: dsPIC33F/PIC24H PLL Block Diagram



Note 1: This specification is temperature dependent. Refer to the **"Electrical Characteristics"** chapter in the specific device data sheet for the exact value.

For PLL operation, the Phase Frequency Detector (PFD) input frequency and Voltage Controlled Oscillator (VCO) output frequency must meet the following requirements:

- The PFD input frequency (FREF) must be in the range of 0.8-8.0 MHz
- The VCO output frequency (FVCO) must be in the range of 100-200 MHz

The PLL Phase Detector Input Divider Select bits (PLLPRE<4:0>) in the Clock Divisor register (CLKDIV<4:0>) specify the input divider ratio (N1), which is used to scale down the input clock (FIN) to meet the PFD input frequency range of 0.8-8 MHz.

The PLL Feedback Divisor bits (PLLDIV<8:0>) in the PLL Feedback Divisor register (PLLFBD<8:0>) specify the divider ratio (M), which scales down the FVCO for feedback to the PFD. The FVCO is 'M' times the input FREF.

The PLL VCO Output Divider Select bits (PLLPOST<1:0>) in the Clock Divisor register (CLKDIV<7:6>) specify the divider ratio (N2) to limit the system clock frequency (FOSC) to 80 MHz.

Equation 39-3 shows the relationship between the FIN and the FOSC.

Equation 39-3: Fosc Calculation

$$FOSC = FIN \times \left(\frac{M}{N1 \times N2}\right) = FIN \times \left(\frac{(PLLDIV + 2)}{(PLLPRE + 2) \times 2(PLLPOST + 1)}\right)$$

Where:

$N1 = PLLPRE + 2$

$N2 = 2 \times (PLLPOST + 1)$

$M = PLLDIV + 2$

Equation 39-4 shows the relation between the FIN and the FVCO.

Equation 39-4: Fvco Calculation

$$FVCO = FIN \times \left(\frac{M}{N1}\right) = FIN \times \left(\frac{(PLLDIV + 2)}{(PLLPRE + 2)}\right)$$

39.7.1 Input Clock Limitation at Start-up for PLL Mode

Table 39-6 lists the default values of the PLL Prescaler, PLL Postscaler, and PLL Feedback Divisor Configuration bits at a POR.

Table 39-6: PLL Mode Defaults

Register	Bit Field	Value at POR	PLL Divider Ratio
CLKDIV<4:0>	PLLPRE<4:0>	00	N1 = 2
CLKDIV<7:6>	PLLPOST<1:0>	01	N2 = 4
PLLFBD<8:0>	PLLDIV<8:0>	000110000	M = 50

Given these Reset values, the following equations demonstrate the relationship between the FIN and the FREF, and the FVCO and the FOSC, at a POR.

Equation 39-5: FREF at a POR

$$FREF = FIN\left(\frac{1}{N1}\right) = 0.5(FIN)$$

Equation 39-6: FVCO at a POR

$$Fvco = FIN\left(\frac{M}{N1}\right) = FIN\left(\frac{50}{2}\right) = 25(FIN)$$

Equation 39-7: FOSC at a POR

$$FOSC = FIN\left(\frac{M}{N1 \cdot N2}\right) = 6.25(FIN)$$

In accordance with the preceding equations at a POR, the FIN to the PLL module must be limited to 4 MHz < FIN < 8 MHz to comply with the FVCO requirement (100M < FVCO < 200M), if the default values of PLLPRE, PLLPOST, and PLLDIV are used.

The POSC can support the following input frequency ranges, which are not within the frequency limit required (4 MHz < FIN < 8 MHz) at a POR:

- POSC in XT mode supports: 3-10 MHz crystal
- POSC in HS mode supports: 10-40 MHz crystal
- POSC in EC mode supports: 0.8-64 MHz input

To use the PLL when the input frequency is not within the 4-8 MHz range, follow these procedure:

1. Power-up the device with the Internal FRC Oscillator without the PLL or the POSC without the PLL.
2. Change the PLLDIV, PLLPRE and PLLPOST bit values, based on the input frequency, to meet these PLL requirements:
   - The PFD input frequency (FREF) must be in the range of 0.8-8.0 MHz
   - The VCO output frequency (FVCO) must be in the range of 100-200 MHz
3. Switch the clock to the PLL mode in software.

39.7.2 PLL Lock Status

Whenever the PLL input frequency, the PLL prescaler, or the PLL feedback divisor is changed, the PLL requires a finite amount of time (TLOCK) to synchronize to the new settings.

TLOCK is applied when the PLL is selected as the clock source at a POR, or during a clock switching operation. The value of TLOCK is relative to the time at which the clock is available to the PLL input. For example, with the POSC, TLOCK starts after the OST delay. Refer to **39.5.1 "Oscillator Start-up Time"** for more information about oscillator start-up delay. Refer to the specific device data sheet for information about typical TLOCK values.

The PLL Lock Status bit (LOCK) in the Oscillator Control register (OSCCON<5>) is a read-only bit that indicates the Lock status of the PLL. The LOCK bit is cleared at a POR and on a clock-switch operation, if the PLL is selected as the destination clock source. The LOCK bit remains clear when any clock source not using the PLL is selected.

After a clock switch event in which the PLL is enabled, wait for the LOCK bit to be set before executing the code.

Note:	The PLLPRE bits and PLLDIV bits should not be changed when operating in PLL mode. Clock-switch to a non-PLL mode (e.g., Internal FRC), to make the necessary changes, and then clock switch back to the PLL mode.

39.7.2.1 SETUP FOR USING PLL WITH POSC

The following process can be used to set up the PLL to operate the device at 40 MIPS with a 10 MHz external crystal:

1. To execute instructions at 40 MHz, ensure that the required system clock frequency is FOSC = 2 x FCY = 80 MHz.
2. Ensure that the default Reset values of PLLPRE, PLLPOST and PLLDIV meet the PLL and user requirements.
3. If the PLL and user requirements are met, configure the FNOSC bits (FOSCSEL<2:0>) to select the POSC with PLL at a POR. If the PLL and user requirements are not met, perform the following steps:
   a) Select the PLL postscaler to meet the VCO output frequency requirement (100 MHz < FVCO < 200 MHz).
   b) Select the PLL prescaler to meet the PFD input frequency requirement (0.8 MHz < FREF < 8 MHz).
   c) Select the PLL feedback divisor to generate the required VCO output frequency based on the PFD input frequency.
   d) Configure the FNOSC bits (FOSCSEL<2:0>) to select a clock source without the PLL (e.g., Internal FRC) at a POR.
   e) In the main program, change the PLL prescaler, PLL postscaler, and PLL feedback divisor values to the values derived in the previous steps. Then, perform a clock switch to the PLL mode.

Example 39-1 demonstrates the code for using PLL with the POSC. See **39.12 "Clock Switching"** for a clock-switching code example.

Example 39-1: Code Example for Using the PLL with the 10 MHz Posc Crystal

```
_FOSCSEL(FNOSC_FRC & IESO_OFF);   // Internal FRC start-up without PLL,
                                  // no Two Speed Start-up
_FOSC(FCKSM_CSECMD & OSCIOFNC_OFF & POSCMD_XT);  // Clock switch enabled,
                                                 // Primarly Oscillator XT
_FWDT(FWDTEN_OFF);                // Watchdog Timer disabled
_FPOR(PPWRT_PWR128);              // Power-up Timer enabled 128 ms
_FICD(JTAGEN_OFF);                // Disable JTAG

int main()
{

// Configure PLL prescaler, PLL postscaler, PLL divisor
PLLFBD=30;            // M = 32
CLKDIVbits.PLLPOST=0;  // N2 = 2
CLKDIVbits.PLLPRE=0;   // N1 = 2

// Initiate Clock Switch to Primary Oscillator with PLL (NOSC = 0b011)
__builtin_write_OSCCONH(0x03);
__builtin_write_OSCCONL(OSCCON | 0x01);

// Wait for Clock switch to occur
while (OSCCONbits.COSC != 0b011);

// Wait for PLL to lock
while(OSCCONbits.LOCK!=1) {};

}
```

39.7.2.2 SETUP FOR USING PLL WITH 7.37 MHz INTERNAL FRC

The following process can be used to set up the PLL to operate the device at 40 MIPS with a 7.37 MHz Internal FRC.

1. To execute instructions at 40 MHz, ensure that the system clock frequency is FOSC = 2 x FCY = 80 MHz.
2. Ensure that the default Reset values of PLLPRE, PLLPOST and PLLDIV meet the PLL and user requirements.
3. If the PLL and user requirements are met, configure the FNOSC bits (FOSCSEL<2:0>) to select the POSC with PLL at a POR. If the PLL and user requirements are not met, perform the following steps:
   a) Select the PLL postscaler to meet the VCO output frequency requirement (100 MHz < FVCO < 200 MHz).
   b) Select the PLL prescaler to meet the PFD input frequency requirement (0.8 MHz < FREF < 8 MHz).
   c) Select the PLL feedback divisor to generate the required VCO output frequency based on the PFD input frequency.
   d) Configure the FNOSC bits (FOSCSEL<2:0>) to select a clock source without PLL (e.g., the Internal FRC Oscillator) at a POR.
   e) In the main program, change the PLL prescaler, PLL postscaler, and PLL feedback divisor values to meet the PLL and user requirements. Then, perform a clock switch to the PLL mode.

Example 39-2 demonstrates the code for using the PLL with a 7.37 MHz Internal FRC. See **39.12 "Clock Switching"** for a clock switching code example.

Example 39-2: Code Example for Using the PLL with the 7.37 MHz Internal FRC Oscillator

```
_FOSCSEL(FNOSC_FRC & IESO_OFF);   // Internal FRC start-up without PLL,
                                  // no Two Speed Start-up
_FOSC(FCKSM_CSECMD & OSCIOFNC_OFF & POSCMD_XT);  // Clock switch enabled,
                                                 // Primarly Oscillator XT
_FWDT(FWDTEN_OFF);                // Watchdog Timer disabled
_FPOR(PPWRT_PWR128);              // Power-up Timer enabled 128 ms
_FICD(JTAGEN_OFF);                // Disable JTAG

int main()
{

// Configure PLL prescaler, PLL postscaler, PLL divisor
PLLFBD = 63;           // M = 65
CLKDIVbits.PLLPOST=0;  // N2 = 2
CLKDIVbits.PLLPRE=1;   // N1 = 3

// Initiate Clock Switch to Internal FRC with PLL (NOSC = 0b001)
__builtin_write_OSCCONH(0x01);
__builtin_write_OSCCONL(OSCCON | 0x01);

// Wait for Clock switch to occur
while (OSCCONbits.COSC != 0b001);

// Wait for PLL to lock
while(OSCCONbits.LOCK!=1) {};

}
```

39.8 SECONDARY OSCILLATOR (SOSC)

The Secondary Oscillator (SOSC) enables a 32.768 kHz crystal oscillator to be attached to the dsPIC33F/PIC24H device as a secondary crystal clock source for low-power operation. It uses the SOSCI and SOSCO pins. The SOSC can also drive Timer1 for Real-Time Clock (RTC) applications.

Note: The SOSC is sometimes referred to as the Low-Power Secondary Oscillator due to it's low-power capabilities. However, this oscillator should not be confused with the LPRC Oscillator.

39.8.1 SOSC for System Clock

The SOSC is enabled as the system clock in the following conditions:

- Initial Oscillator Source Selection Configuration bits (FNOSC<2:0>) in the Oscillator Source Selection register (FOSCSEL<2:0>) are appropriately set to select the SOSC at a POR
- The user application initiates a clock switch to the SOSC for low-power operation

If the SOSC is not being used to provide the system clock, or if the device enters Sleep mode, it is disabled to save power.

39.8.2 SOSC Start-up Delay

When the SOSC is enabled, it takes a finite amount of time to start oscillating. Refer to **39.5.1 "Oscillator Start-up Time"** for details.

39.8.3 Continuous SOSC Operation

Optionally, the SOSC can run continuously. The SOSC is always enabled, if the Secondary Oscillator Enable bit (LPOSCEN) is set in the Oscillator Control register (OSCCON<1>).

There are two reasons to have the SOSC running:

1. Allowing the SOSC to run continuously facilitates a fast switch to the 32 kHz system clock for lower-power operation. Returning to the faster main oscillator would require start-up time if it is a crystal-type source (see **39.5.1 "Oscillator Start-up Time"**).
2. If Timer1 is being used as an RTC, the oscillator must be on.

Note: In Sleep mode, all clock sources (POSC, Internal FRC Oscillator, and LPRC Oscillator) are shut down, with the exception of the SOSC and LPRC under certain conditions. If the Watchdog Timer is enabled, the LPRC is always active, even in Sleep mode. The SOSC can be active in Sleep mode if the Secondary Oscillator Enable bit (LPOSCEN) is set in the Oscillator Control register (OSCCON<1>).

39.9 LOW-POWER RC (LPRC) OSCILLATOR

The Low-Power RC (LPRC) Oscillator provides a nominal clock frequency of 32 kHz. The LPRC Oscillator is the clock source for the Power-up Timer (PWRT), Watchdog Timer (WDT), and Fail-Safe Clock Monitor (FSCM) circuits. It can also be used to provide a low-frequency clock source option for the device in those applications where power consumption is critical and timing accuracy is not required.

Note:	The clock frequency of the LPRC Oscillator will vary depending on the device voltage and operating temperature. Refer to the **"Electrical Characteristics"** in the specific device data sheet for details.

39.9.1 LPRC Oscillator for System Clock

The LPRC Oscillator is selected as the system clock in the following conditions:

- Initial Oscillator Source Selection bits (FNOSC<2:0>) in the Oscillator Source Selection register (FOSCSEL<2:0>) are appropriately set to select the LPRC Oscillator at a POR
- The user application initiates a clock switch to the LPRC Oscillator for low-power operation

39.9.2 Enabling the LPRC Oscillator

The LPRC Oscillator is the clock source for the PWRT, WDT, and FSCM.

The LPRC Oscillator is enabled at a POR, if the POR Timer Value Select bits (FPWRT)in the POR Configuration Fuse register (FPOR<2:0>) are set.

The LPRC Oscillator remains enabled under these conditions:

- FSCM is enabled
- WDT is enabled
- LPRC Oscillator is selected as the system clock

If none of these conditions is true, the LPRC Oscillator shuts off after the PWRT expires. The LPRC Oscillator is shut off in Sleep mode.

Note:	The LPRC Oscillator runs in Sleep mode only if the WDT is enabled. Under all other conditions, the LPRC Oscillator is disabled in Sleep mode.

39.9.3 LPRC Oscillator Start-up Delay

The LPRC Oscillator starts up instantly; unlike a crystal oscillator, which can take several milliseconds to begin oscillation.

39.10 AUXILIARY OSCILLATOR (AOSC)

The Auxiliary Oscillator (AOSC) can be used for peripherals that need to operate at a frequency unrelated to the system clock, such as a Digital-to-Analog Converter (DAC).

The AOSC can use one of the following as its clock source:

- Crystal (XT mode) – crystal and ceramic resonators in the range of 3-10 MHz
- High-Speed Crystal (HS mode) – crystals in the range of 10-40 MHz
  The external crystal is connected to the SOSCI and SOSCO pins.
- External Clock (EC mode) – an external clock signal (up to 64 MHz)
  The external clock signal is applied directly to the SOSCI pin.

39.10.1 Enabling the AOSC

To enable the Auxiliary Oscillator mode and External Oscillator mode, the appropriate Auxiliary Oscillator Mode bits (AOSCMD<1:0>) must be selected in the Auxiliary Clock Control register (ACLKCON<12:11>).

These bits allow for four oscillator-mode settings, as shown in Table 39-7. Once the mode has been selected, set the Select Auxiliary Clock Source for Auxiliary Clock Divider bit (SELACLK) in the Auxiliary Clock Control register (ACLKCON<13>) to use the AOSC as the clock reference.

Table 39-7: AOSC and External Oscillator Mode Select Settings

AOSCMD<1:0> Bit Value	Oscillator Mode Setting
11	EC (External Clock) Mode Select
10	XT (Crystal) Oscillator Mode Select
01	HS (High-Speed) Oscillator Mode Select
00	AOSC Disabled (default setting)

Note: By default, the DAC module is clocked by the Internal FRC Oscillator with the PLL. To use the POSC as the clock source, set the following bits in the ACLKCON register:

- ASRCSEL (selects the POSC for the reference clock)
- SELACLK (enables the reference clock)

39.10.2 Auxiliary Clock Output Divider

The Auxiliary Clock Output Divider bits (APSTSCLR<2:0>) in the Auxiliary Clock Control register (ACLKCON<10:8>) divide the auxiliary clock, which allows a lower frequency to be chosen. These bits allow for eight postscaler settings, from 1:1 to 1:256, as shown in Table 39-8.

Table 39-8: Auxiliary Clock Output Divider Settings

APSTSCLR<2:0> Bit Value	AOSC Setting
111	Divide by 1
110	Divide by 2
101	Divide by 4
100	Divide by 8
011	Divide by 16
010	Divide by 32
001	Divide by 64
000	Divide by 256 (default setting)

39.11 FAIL-SAFE CLOCK MONITOR (FSCM)

The Fail-Safe Clock Monitor (FSCM) allows the device to continue operating when an oscillator failure occurs. FSCM function is enabled by programming the Clock Switching Mode Configuration bits (FCKSM<1:0>) in the Oscillator Configuration register (FOSC<7:6>) during device programming. When the FSCM is enabled (FCKSM<1:0> = 00), the LPRC Oscillator runs continuously, except during Sleep mode.

The FSCM monitors the system clock. If FSCM does not detect a system clock within a specific period of time (typically 2 ms, 4 ms maximum), it generates a clock failure trap and switches the system clock to the Internal FRC Oscillator. At that point, the user application can either attempt to restart the oscillator or execute a controlled shutdown.

Note:	The FSCM does not wake-up the device if the clock fails while the device is in Sleep mode.

The FSCM module takes the following actions when it switches to the Internal FRC Oscillator:

- Current Oscillator Selection bits (COSC<2:0>) in the Oscillator Control register (OSCCON<14:12>) are loaded with '000' (Internal FRC Oscillator)
- Clock Fail Detect bit (CF) in the Oscillator Control register (OSCCON<3>) is set to indicate clock failure
- Oscillator Switch Enable Control bit (OSWEN) in the Oscillator Control register (OSCCON<0>) is cleared to cancel any pending clock switches
- The Interrupt Status bit, OSCFAIL (INTCON1<1>), is set and must be cleared by user software
- An oscillator fail trap interrupt is taken

39.11.1 FSCM Delay

The FSCM monitors the system clock for activity after the system clock is ready and the nominal delay (TFSCM) has elapsed.

The FSCM delay is applied when the FSCM is enabled, and the POSC or the SOSC is selected as the system clock.

Refer to **Section 8. "Reset"** (DS70192) for additional information.

Note:	Please refer to the **"Electrical Characteristics"** section of the specific device data sheet for TFSCM values.

39.11.2 FSCM and WDT

The FSCM and the WDT use the LPRC Oscillator as their time base. In the event of a clock failure, the WDT is unaffected and continues to run on the LPRC Oscillator.

39.12 CLOCK SWITCHING

Clock switching can be initiated as a result of the hardware event or a software request. Typical scenarios include:

- Two-Speed Start-Up sequence on a POR, which initially uses the Internal FRC Oscillator for quick start-up, and then automatically switches to the selected clock source when the clock is ready
- FSCM automatically switches to Internal FRC Oscillator on a clock failure
- User application software requests clock switching by setting the OSWEN bit (OSCCON<0>), causing the hardware to switch to the clock source selected by the NOSC bits (OSCCON<10:8>) when the clock is ready

In each of these cases, the clock switch event ensures that the proper make-before-break sequence is executed. That is, the new clock source must be ready before the old clock is deactivated, and code must continue to execute as clock switching occurs.

With few limitations, applications are free to switch between any of the four clock sources (the POSC, SOSC, FRC and LPRC) that are controlled by software. To limit the possible side effects that could result from this flexibility, dsPIC33F/PIC24H devices have a safeguard lock built into the switch process. That is, the OSCCON register is write-protected during clock switching.

39.12.1 Enabling Clock Switching

The Clock Switching Mode Configuration bits (FCKSM<1:0>) in the Oscillator Configuration register (FOSC<7:6>) must be programmed to enable clock switching and the FSCM (see Table 39-9).

Table 39-9: Configurable Clock Switching Modes

FCKSM<1:0> Values	Clock Switching Configuration	FSCM Configuration
1x	Disabled	Disabled
01	Enabled	Disabled
00	Enabled	Enabled

The first bit determines whether clock switching is enabled (‘0’) or disabled (‘1’). The second bit determines whether the FSCM is enabled (‘0’) or disabled (‘1’). The FSCM can only be enabled if clock switching is also enabled. If clock switching is disabled (‘1’), the value of the second bit is irrelevant.

39.12.2 Clock Switch Sequence

The recommended process for a clock switch includes the following steps:

1. Read the COSC bits (OSCCON<14:12>) to determine the current oscillator source (if this information is relevant to the application).
2. Execute the unlock sequence, allowing a write to the high byte of the OSCCON register.
3. Write the appropriate value to the NOSC Control bits (OSCCON<10:8>) for the new oscillator source.
4. Execute the unlock sequence, allowing a write to the low byte of the OSCCON register.
5. Set the OSWEN bit (OSCCON<0>) to initiate the oscillator switch.

After those steps have been completed, the clock switch logic executes the following actions:

1. The clock switching hardware compares the values of the COSC<2:0> Status bits in the Oscillator Control register (OSCCON <14:12>) with the new values of the NOSC<2:0> Control bits (OSCCON<10:8>). If the values match, the clock switch is a redundant operation, the OSWEN bit (OSCCON<0>) is cleared automatically, and the clock switch is aborted.
2. If a valid clock switch has been initiated, the PLL Lock Status bit (OSCCON<5>) and the Clock Fail Status bit (OSCCON<3>) are cleared.
3. The new oscillator is turned on by the hardware (if it is not currently running). If a crystal oscillator (POSC or SOSC) must be turned on, the hardware waits for TOSCD until the crystal starts oscillating and TOST expires. If the new clock source uses the PLL, the hardware waits until a PLL lock is detected (OSCCON<5> = 1).

4. The hardware waits for the new clock source to stabilize and then performs the clock switch.
5. The hardware clears the OSWEN bit (OSCCON<0>) to indicate a successful clock transition. In addition, the values of the NOSC<2:0> bits (OSCCON<10:8>) are transferred to the COSC<2:0> Status bits (OSCCON<14:12>).
6. The old clock source is turned off at this time, with the exception of the LPRC Oscillator (if the WDT or FSCM is enabled) or the SOSC (if LPOSCEN remains set). The timing of the transition between clock sources is shown in Figure 39-9.

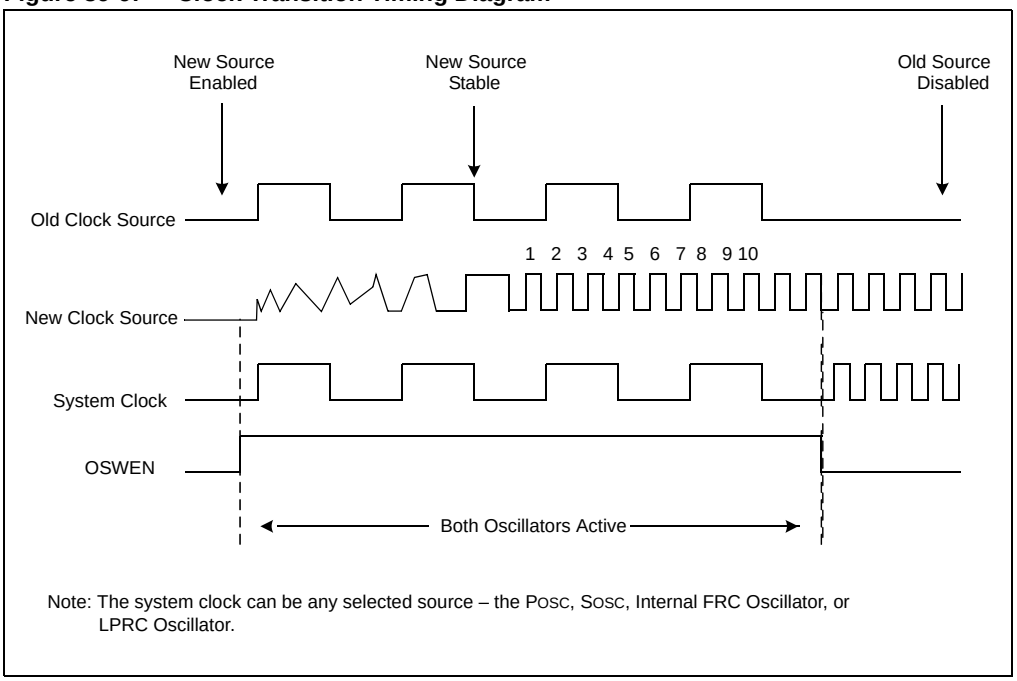
Note 1: Clock switching between XT, HS and EC Primary Oscillator modes is not possible without reprogramming the device.

2: Direct clock switching between PLL modes is not possible. For example, clock switching should not occur between the POSC with PLL, and the Internal FRC Oscillator with PLL.

3: Setting the CLKLOCK bit (OSCCON<7>) prevents clock switching when clock switching is enabled and the FSCM is disabled by the FCKSM Configuration bits (FOSC<7:6> = 01). The CLKLOCK bit (OSCCON<7>) cannot be cleared when it has been set by software; it clears on a POR.

4: The processor continues to execute code throughout the clock switching sequence. Timing-sensitive code should not be executed during this time.

Figure 39-9: Clock Transition Timing Diagram



Note: The system clock can be any selected source – the POSC, SOSC, Internal FRC Oscillator, or LPRC Oscillator.

A recommended code sequence for a clock switch includes the following actions:

1. Disable interrupts during the OSCCON register unlock-and-write sequence.
2. Execute the unlock sequence for the OSCCON high byte.
   Perform the following steps in two back-to-back instructions:
   - Write 0x78 to OSCCON<15:8>
   - Write 0x9A to OSCCON<15:8>
3. In the instruction that follows the unlock sequence, write the new oscillator source to the NOSC<2:0> Control bits in the Oscillator Control register (OSCCON<10:8>).
4. Execute the unlock sequence for the OSCCON low byte.
   Perform the following steps in two back-to-back instructions:
   - Write 0x46 to OSCCON<7:0>
   - Write 0x57 to OSCCON<7:0>
5. In the instruction immediately following the unlock sequence, set the OSWEN bit (OSCCON<0>).
6. Continue to execute code that is not clock-sensitive (optional).
7. Check to see whether the OSWEN bit (OSCCON<0>) is '0'. If it is, the switch is successful.

Note: MPLAB® C Compiler for PIC24 MCUs and dsPIC DSCs provides the following built-in C language functions for unlocking and writing to the OSCCON register:

```
__builtin_write_OSCCONH(value)
__builtin_write_OSCCONL(OSCCON | value)
```

See MPLAB C Compiler Help for more information.

Example 39-3 demonstrates the code sequence for unlocking the OSCCON register, and switching from the Internal FRC Oscillator with PLL clock to the LPRC Oscillator clock source.

Example 39-3: Code Example for Clock Switching

```
;Place the New Oscillator Selection (NOSC=0b101) in W0
MOV #0x5, WREG
;OSCCONH (high byte) Unlock Sequence
MOV     #OSCCONH, w1
MOV     #0x78, w2
MOV     #0x9A, w3
MOV.B   w2, [w1]    ; Write 0x78
MOV.B   w3, [w1]    ; Write 0x9A

;Set New Oscillator Selection
MOV.B   WREG, OSCCONH

;OSCCONL (low byte) Unlock Sequence
MOV     #OSCCONL, w1
MOV     #0x46, w2
MOV     #0x57, w3
MOV.B   w2, [w1]    ; Write 0x46
MOV.B   w3, [w1]    ; Write 0x57

; Enable Clock Switch
BSET    OSCCON, #0 ; Request Clock Switching by Setting OSWEN bit
wait:
btsc OSCCONL, #OSWEN
bra wait
```

39.12.3 Clock Switching Consideration

When planning an application that will include clock switching, the following issues could affect the code design:

- The OSCCON unlock sequence is extremely timing critical. The OSCCON register byte is only writable for one instruction cycle following the sequence. Some high-level languages, such as C, may not preserve the timing-sensitive sequence of instructions when compiled. When clock switching is required for an application written in a high-level language, create the routine in assembly code and link it to the application, and then call it as a function, when it is required.
- If the destination clock source is a crystal oscillator, the clock switch time will be dominated by the oscillator start-up time.
- If the new clock source does not start, or is not present, the clock switching hardware will continue to run from the current clock source. The software can detect this situation because the OSWEN bit (OSCCON<0>) remains set indefinitely.
- If the new clock source uses the PLL, a clock switch will not occur until the lock has been achieved. The software can detect a loss of the PLL lock because the LOCK bit (OSCCON<5>) is cleared and the OSWEN bit (OSCCON<0>) is set.
- Switching to a low-frequency clock source, such as the SOSC, will result in slow device operation.

39.12.4 Aborting a Clock Switch

If a clock switch does not complete, the clock switch logic can be reset by clearing the OSWEN bit (OSCCON<0>). When OSWEN is cleared, the clock switch process is aborted, the Oscillaot Start Time (if applicable) is stopped and reset, and the PLL (if applicable) is stopped.

Typical assembly code for aborting a clock switch is shown in Example 39-4. A clock switch procedure can be aborted at any time. A clock switch that is already in progress can also be aborted by performing a second clock switch.

Example 39-4: Aborting a Clock Switch

```
MOV     #OSCCON,W1      ; Pointer to OSCCON
MOV.b   #0x46,W2        ; First unlock code
MOV.b   #0x57,W3        ; second unlock code
MOV.b   W2, [W1]        ; Write first unlock code
MOV.b   W3, [W1]        ; Write second unlock code
BCLR    OSCCON,#OSWEN   ; ABORT the switch
```

39.12.5 Entering Sleep Mode During a Clock Switch

If the device enters Sleep mode during a clock switch operation, the clock switch operation is aborted. The processor keeps the old clock selection, and the OSWEN bit is cleared. The PWRSAV instruction is then executed normally.

It is particularly useful to perform a clock switch to the Internal FRC Oscillator before entering Sleep mode, as this ensures fast wake-up from Sleep mode.

39.13 TWO-SPEED START-UP

The Internal External Start-up Option Configuration bit (IESO) in the Oscillator Source Selection register (FOSCSEL<7>) specifies whether to start the device with a user-selected oscillator source; or to initially start with the Internal FRC Oscillator and then automatically switch to the user-selected oscillator. If the IESO bit is set to '1', the device will always power-up on the Internal FRC Oscillator, regardless of the other oscillator source settings (FOSCSEL<2:0>). The device then automatically switches to the specified oscillator.

Unless FSCM is enabled, the Internal FRC Oscillator is automatically turned off immediately after the clock switch is completed. The Two-Speed Start-Up option is a faster way to get the device up and running, and works independently of the state of the Clock-switching mode bits (FCKSM<1:0>) in the Oscillator Configuration register (FOSC<7:6>).

Two-Speed Start-Up is particularly useful when an external oscillator, a POSC or SOSC (which have a longer start-up time), is selected by the FOSCSEL Configuration bits (FOSC<2:0>).

As an internal RC oscillator, the Internal FRC Oscillator clock source is available almost immediately after a POR. With Two-Speed Start-Up, the device starts executing code in its default oscillator configuration, the Internal FRC Oscillator. The device continues to operate in this mode until the specified external oscillator source becomes stable, then it automatically switches to that source.

User code can check which clock source is currently providing the device clocking by checking the status of the COSC bits (OSCCON<14:12>) against the NOSC bits (OSCCON<10:8>). If these two sets of bits match, the clock switch has been completed successfully and the device is running from the intended clock source.

Note:	Two-Speed Start-Up is redundant if the selected device clock source is the Internal FRC Oscillator.

39.14 REGISTER MAPS

Table 39-10 maps the bit functions for the Oscillator Special Function Control registers. Table 39-11 maps the bit functions for the Oscillator Configuration registers.

Table 39-10: Oscillator Special Function Control Registers

File Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
OSCCON	—	COSC<2:0>			—	NOSC<2:0>			CLKLOCK	IOLOCK(2)	LOCK	—	CF	—	LPOSCEN	OSWEN	7700(1)
CLKDIV	ROI	DOZE<2:0>			DOZEN	FRCDIV<2:0>			PLLPOST<1:0>		—	PLLPRE<4:0>					3040
PLLFBD	—	—	—	—	—	—	—	PLLDIV<8:0>									0030
OSCTUN	—	—	—	—	—	—	—	—	—	—	TUN<5:0>						0000
ACLKCON	—	—	SELACLK	AOSCMD<1:0>		APSTSCLR<2:0>			ASRCSEL	—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note 1: OSCCON register Reset values are dependent on the FOSCSEL Configuration bits and the type of Reset.
2: The IOLOCK bit is not available on all dsPIC33F/PIC24H devices. Consult the specific device data sheet for more information.

Table 39-11: Oscillator Configuration Registers

File Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FOSCSEL	—	—	—	—	—	—	—	—	IESO	—	—	—	—	FNOSC<2:0>		
FOSC	—	—	—	—	—	—	—	—	FCKSM<1:0>		IOL1WAY(1)	—	—	OSCIOFNC	POSCMD<1:0>	

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note 1: The IOL1WAY bit is not available on all dsPIC33F/PIC24H devices. Consult the specific device data sheet for more information.

39.15 RELATED APPLICATION NOTES

This section lists application notes that pertain to this section of the manual. These application notes may not be written specifically for the dsPIC33F/PIC24H product families, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes that are related to the Oscillator (Part III) module include:

Title	Application Note #
PIC® Microcontroller Oscillator Design Guide	AN588
Low-Power Design using PIC® Microcontrollers	AN606
Crystal Oscillator Basics and Crystal Selection for rfPIC® MCU and PIC® MCU Devices	AN826

Note: Please visit the Microchip web site (www.microchip.com) for additional Application Notes and code examples for the dsPIC33F/PIC24H families of devices.

39.16 REVISION HISTORY

Revision A (October/November 2007)

This is the initial release of this document.

Revision B (September 2008)

This revision incorporates the following updates:

- Figures:
  - Updated the label PLLCLK with FVCO(1) in Figure 39-1
- Notes:
  - Added Note 1 to refer the FVCO values (see Figure 39-1)
- Registers:
  - The tuned frequencies for bit 5-0 in the OSCTUN: FRC Oscillator Tuning Register have been corrected (see Register 39-6)
- Additional minor corrections such as language and formatting updates are incorporated throughout the document

Revision C (April 2010)

This revision incorporates the following content updates:

Merged the dsPIC33F and PIC24H family reference manual sections titled “Section 39. Oscillator (Part III)”, into this single document

- Registers:
  - Added Notes 1 and 2 to Register 39-3
  - Added Note 2 to Register 39-4
  - Updated SELACLK bit description (see Register 39-7)
- Figures:
  - Updated Figure 39-1
  - Updated Figure 39-3
- Added Note 2 regarding FRC Oscillator Tuning (TUN<5:0>) bits to Internal Fast RC (FRC) Oscillator section (**39.6 “Internal Fast RC (FRC) Oscillator”**)
- Updated code examples (Example 39-1, Example 39-2 and Example 39-3)
- Additional minor corrections such as language and formatting updates have been incorporated throughout the document

Revision D (April 2012)

This revision includes the following updates:

- Updated Note 2 in the Clock Pin Function Selection (see Table 39-3)
- Updated the dsPIC33F/PIC24H PLL Block Diagram (see Figure 39-8)
- Minor updates to text and formatting were incorporated throughout the document

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